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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,487	02/10/2004	Ho-Yuan Yu	65860-5002-US	3256

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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
09/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/776,487	YU, HO-YUAN	
	Examiner	Art Unit	
	Khiem D. Nguyen	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *15-20* is/are allowed.

6)☒ Claim(s) *21-24 and 26-34* is/are rejected.

7)☒ Claim(s) *25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

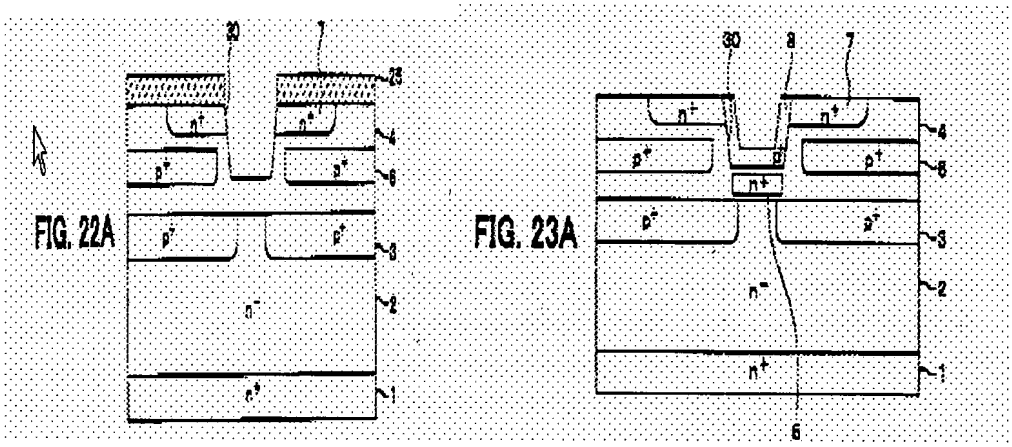
Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 21-24 and 26-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar et al. (U.S. Pub. 2002/0167011).

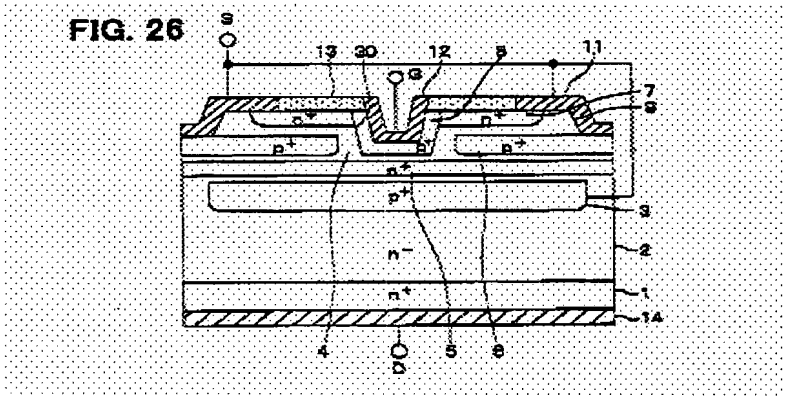
In re claim 21, **Kumar** discloses a method for fabricating a dual gate structure for a field effect transistor (FET), the method comprising: in sequence, etching a gate trench 30 in a surface of a semiconductor substrate 1 (page 7, paragraph [0156] and FIG. 22A);



forming a first gate region 8 at the bottom of the gate trench 30 (page 7, paragraph [0160]); implanting a buffer region 5 beneath the first gate region 8 (page 7, paragraph [0158] and FIGS. 22 A and 23A); and

implanting a second gate region 3 beneath the buffer region 5, wherein the second gate region 3 is formed entirely beneath the first gate region 8 (page 7, paragraph [0164] and FIG. 26).

FIG. 26



Kumar, discloses providing a first gate region 8 at the bottom of the gate trench 30, implanting a buffer region 5 beneath the first gate region 8, and implanting a second gate region 3 beneath the buffer region 5 (see Fig. 23A) but does not explicitly show that these steps are performed in sequence as required by the present claimed invention. However, it would have been obvious to one of ordinary skill in the art to form the buffer region and the second gate region after forming the first gate region because selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

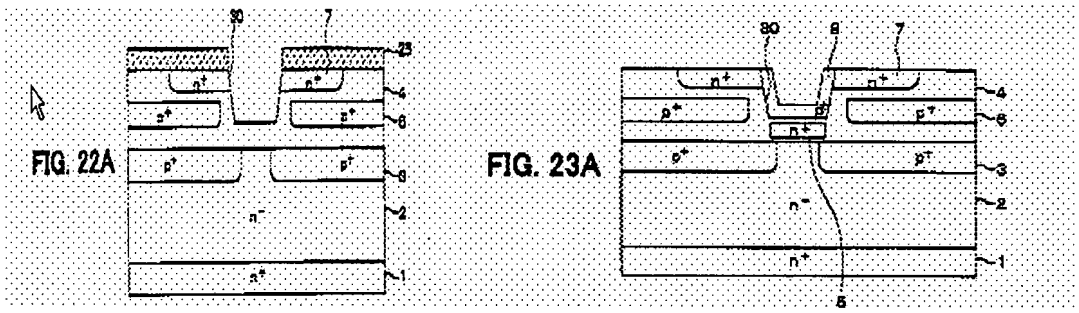
In re claim 22, as applied to claim 21 above, **Kumar** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the first gate region 8 (FIG. 23A).

In re claim 23, as applied to claim 21 above, **Kumar** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the buffer region 5 (FIG. 23B).

In re claim 24, as applied to claim 21 above, **Kumar** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the second gate region 3 (FIG. 26).

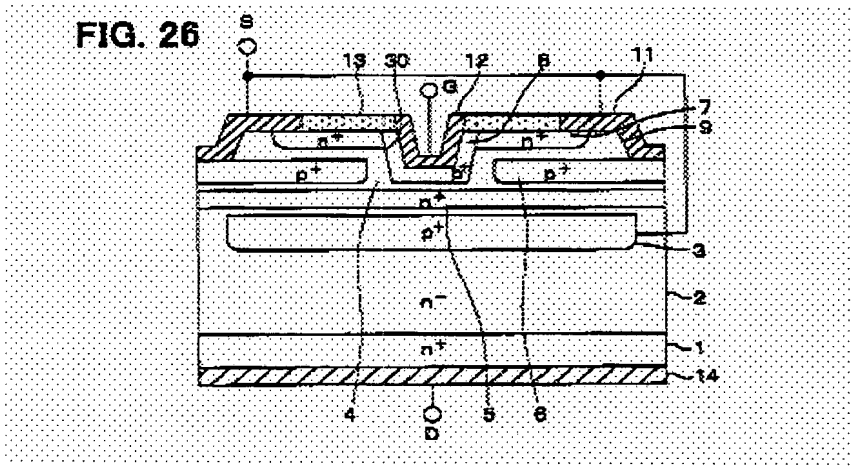
In re claim 26, **Kumar** discloses a method for fabricating a dual gate structure for a field effect transistor (FET), the method comprising: etching a gate trench 30 in a surface of a semiconductor substrate 1 (page 7, paragraph [0156] and FIG. 22A);

forming a first gate region 8 at the bottom of the gate trench 30 (page 7, paragraph [0160]); after forming the first gate region, implanting a buffer region 5 beneath the first gate region 8 (page 7, paragraph [0158] and FIGS. 22A and 23A); and



implanting a second gate region 3 beneath the buffer region 5, wherein the second gate region 3 is formed entirely beneath the first gate region 8 (page 7, paragraph [0164] and FIG. 26).

FIG. 26



Kumar, discloses providing a first gate region 8 at the bottom of the gate trench 30, implanting a buffer region 5 beneath the first gate region 8, and implanting a second gate region 3 beneath the buffer region 5 (see Fig. 23A) but does not explicitly show that the step of implanting a buffer region beneath the first gate region is performed after forming the first gate region as required by the present claimed invention. However, it would have been obvious to one of ordinary skill in the art to perform the step of implanting the buffer region after forming the first gate region because selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

In re claim 27, as applied to claim 26 above, **Kumar** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the first gate region 8 (FIG. 23A).

In re claim 28, as applied to claim 26 above, **Kumar** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the buffer region 5 (FIG. 23B).

In re claim 29, as applied to claim 26 above, **Kumar** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the second gate region 3 (FIG. 26).

In re claim 30, **Kumar** discloses a method for fabricating a dual gate structure for a field effect transistor the method comprising: etching a gate trench 30 in a surface of a semiconductor substrate 1 (page 7, paragraph [0156] and FIG. 22A);

forming a first gate region 8 at the bottom of the gate trench 30 (page 7, paragraph [0160]); implanting a buffer region 5 beneath the first gate region 8 (page 7, paragraph [0158] and FIG. 22A and 23A); and

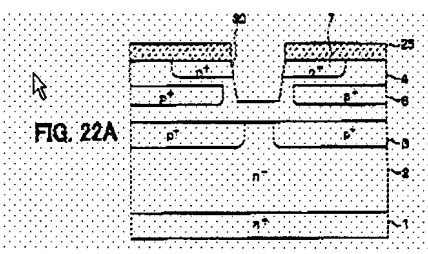


FIG. 22A

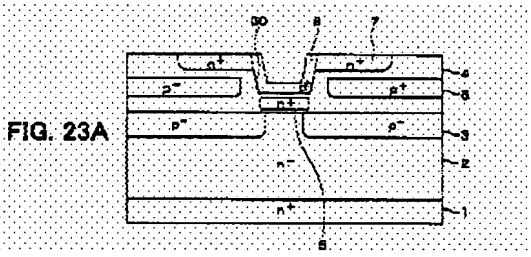
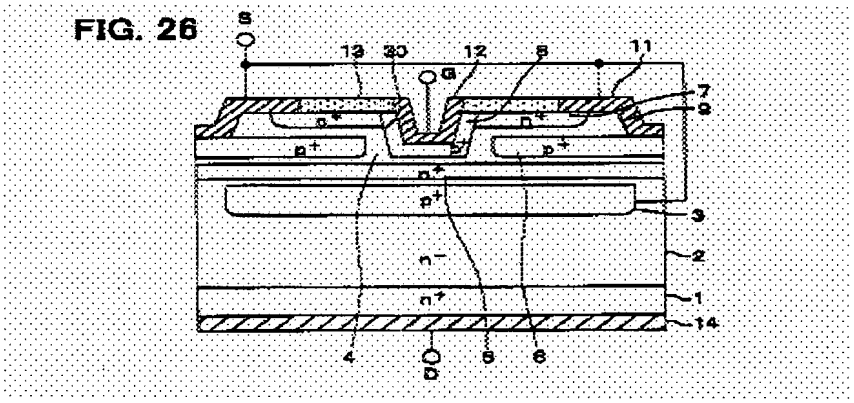


FIG. 23A

after implanting the buffer region 5, implanting a second gate region 3 beneath the buffer region, wherein said second gate region 3 is formed entirely beneath said first gate region 8 (page 7, paragraph [0164] and FIG. 26).

FIG. 26



Kumar, discloses providing a first gate region 8 at the bottom of the gate trench 30, implanting a buffer region 5 beneath the first gate region 8, and implanting a second gate region 3 beneath the buffer region 5 (see Fig. 23A) but does not explicitly show that the step of implanting a second gate region beneath the buffer region is performed after implanting the buffer region as required by the present claimed invention. However, it would have been obvious to one of ordinary skill in the art to perform the step of implanting a second gate region beneath the buffer region after implanting the buffer region because selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

In re claim 31, as applied to claim 30 above, **Kumar** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the first gate region 8 (FIG. 23A).

In re claim 32, as applied to claim 30 above, **Kumar** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the buffer region 5 (FIG. 23B).

In re claim 33, as applied to claim 30 above, **Kumar** discloses all claimed limitations including the limitation wherein the method further comprising forming a sidewall spacer to establish a width of the second gate region 3 (FIG. 26).

In re claim 34, as applied to claim 30 above, **Kumar** discloses all claimed limitations including the limitation wherein the method further comprising forming a first sidewall spacer to establish a width of the buffer region 5, and forming a second sidewall

spacer to establish a width of the second gate region 3, wherein the second sidewall spacer is thicker than the first sidewall spacer (FIG. 26).

Allowable Subject Matter

3. Claims 15-20 were previously allowed over prior art of record as indicated in Office Action mailed on November 13th, 2006.

4. Claim 25 was previously objected to as indicated in Office Action mailed on November 13th, 2006 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Applicants' Amendment and Arguments

5. Applicant's arguments filed July 12th, 2007 have been fully considered but they are not persuasive.

Applicant contends that it would be impossible to implant the first gate area 3 and the field enhanced area 5 having the profiles shown in FIG. 26 of Kumar et al. (U.S. Pub. 2002/0167011), herein known as Kumar. Applicant further suggests that the third gate area 8 would inevitably block and disrupt the implantation steps of forming the two areas 3 and 5 beneath the area 8. Therefore, the Applicant concluded that, changing the order of processing steps as taught by Kumar would produce a semiconductor device with unexpected results, which cannot satisfy the intended purpose as described in Kumar.

In response to Applicant's contention that it would be impossible to implant the first gate area 3 and the field enhanced area 5 having the profiles shown in FIG. 26 of Kumar, Examiner respectfully disagrees.

It is respectfully submitted that the Applicant's claimed invention, as currently presented does not clearly defined a specific profiles including (i.e., shape, dimension, doping concentration, implant energy level, etc...) of the gate and buffer regions. Examiner notes that the claims are given the broadest reasonable interpretation. Therefore, by reversing selection of order of implanting steps of Kumar would still produce the same semiconductor device as claimed by the Applicant, which includes a trench formed in the substrate, a first gate region at the bottom of the trench, a buffer region beneath the first gate region, and a second gate region beneath the buffer region.

For this reason, Examiner holds the rejection proper.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence

7. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Khiem D. Nguyen whose telephone number is (571) 272-1865. The examiner can normally be reached on Monday-Friday (8:30 AM - 5:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

K.N.
September 20, 2007

Brook Kebede

BROOK KEBEDE
PRIMARY EXAMINER